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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,315	09/01/2000	Robert S. Chau	42390.P4222D2	5699

7590

03/24/2003

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EXAMINER

TRAN, THIEN F

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/654,315

Applicant(s)

CHAU ET AL.

Examiner

Thien Tran

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 30,31 and 33-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 30,31 and 33-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 10-01-2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

### *Claim Objections*

Claim 30 is objected to because of the following informalities: lines 6-7, "the silicide layer" should be --the gate silicide layer--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 30-31, 33, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 5,710,450 of record) in view of Fulford et al. (USPN 5,793,089).

Chau et al. discloses a semiconductor device (Fig. 3F) comprising a silicon gate electrode 306 formed on a gate dielectric 302 formed on a substrate surface, the silicon gate electrode having a first thickness; a gate silicon germanium film 314 formed on the silicon gate electrode, the gate silicon germanium film having a second thickness; a gate silicide layer 320 formed on the gate silicon germanium film, the gate silicide layer

Art Unit: 2811

having a third thickness; a pair of sidewall spacers (310, 318) on opposite sides of the silicon gate electrode, the sidewall spacers having a first height above the substrate surface; a pair of source and drain regions 319 formed on opposite sides of said silicon gate electrode, said source and drain regions having a silicon germanium film 314 formed beneath said substrate surface. Chau et al. does not disclose the first height greater than the sum of the first, second and third thicknesses. Fulford et al. discloses a semiconductor device (Fig. 18) comprising sidewall spacers 132 on opposite sides of the gate electrode having a height extending farther above a top surface of the gate silicide layer 136. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chau et al. structure by forming the first height of the sidewall spacers (310, 318) extending farther above a top surface of the gate silicide layer 320 as taught by Fulford et al. in order to prevent the bridging problems between the gate silicide layer on the gate electrode and a silicide layer on the source and drain regions. As a result, the first height of the sidewall spacers of Chau et al. is greater than the sum of the first, second and third thicknesses.

Regarding claims 31 and 37, the silicon gate electrode 306 is polysilicon.

Regarding claim 33, a source/drain silicide layer 320 is formed on the silicon germanium film 314 of the source and drain regions.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (USPN 5,710,450 of record) in view of Fulford et al. (USPN 5,793,089) as applied to claims 30, 31, 33 above, and further in view of Subbanna (USPN 5,338,698 of record).

Art Unit: 2811

Chau et al. in view of Fulford et al. as described above does not disclose an isolation region having a top surface positioned below the top surface of the silicon germanium film 314 of the source and drain regions. However, forming an isolation region having a top surface coplanar with the substrate surface is known in the art as disclosed by Subbanna. Subbanna discloses an isolation region 32 formed in a substrate having a top surface coplanar with the substrate surface. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chau et al.'s structure by forming an isolation region including a top surface coplanar with the substrate surface as taught by Subbanna in order to provide an improved isolation region that can prevent current leakage past the isolation region to increase the effectiveness of the isolation region for electrically isolating adjacent active devices (field effect transistors) from each other. Since the top surface of the isolation region is coplanar with the substrate surface, the top surface of the isolation region is positioned below the top surface of the silicon germanium film 314 of the source and drain regions.

Regarding claim 35, the top surface of the isolation region is positioned below the silicide layer 320.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

Art Unit: 2811

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt  
March 19, 2003

A handwritten signature in black ink, appearing to read 'Thien Tran', is positioned above the printed name.

Thien Tran  
Patent Examiner  
Technology Center 2800